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06EC74

Seventh Semester B.E. Degree Examination, December 2012
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is digital signal processing? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail. **(09 Marks)**

b. Why signal sampling is required? Explain the sampling process. **(05 Marks)**

c. Define decimation and interpolation process. Explain them using block diagrams and equations. **(06 Marks)**

2 a. Give the structure of a 4×4 Braun multiplier, explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on speed of the multiplier. **(10 Marks)**

b. Explain guard bits in a MAC unit of a DSP. Consider a MAC unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required? **(10 Marks)**

3 a. What is the function of an address generation unit? Explain with the help of a block diagram. **(08 Marks)**

b. Why circular buffers are required in DSP processors? How they are implemented? **(02 Marks)**

c. Explain the barrel shifter of the TMS320C54XX processor with the help of a functional diagram. **(05 Marks)**

d. Explain the direct addressing mode of the TMS320C54XX processor with the help of a block diagram. **(05 Marks)**

4 a. A digital signal processor has a circular buffer with the start and end addresses as 0200h and 0310h. What is the circular buffer size? What would be the new values of address pointer of the above buffer if, in the course of address computation, it gets updated to, i) 0336h ii) 0192h. **(06 Marks)**

b. Show the pipeline operation of the following sequence of instructions if the initial value of AR3 is 80 and the values stored in the memory locations 80, 81, 82 are 1, 2, 3 respectively.

```
LD *AR3+, A
ADD # 1000h, A
STL A, *AR3+
```

(08 Marks)

c. Give the logical block diagram of timer circuit. Explain its operation. **(06 Marks)**

PART – B

5 a. Determine the value of each of the following 16-bit numbers represented using the given Q-notation:

i) 4400h as a Q0 number.
ii) 4400h as a Q15 number.
iii) 4400h as a Q7 number
iv) 4400h as a Q1 number. **(04 Marks)**

b. With the help of a block diagram explain the implementation of an FIR filter in TMS320C54XX processor. Show the memory organization for the filter implementation. **(08 Marks)**

c. What is the drawback of using linear interpolation for implementing interpolation filter? Explain a scheme that overcomes this drawback. **(06 Marks)**

d. How do you obtain the product of two 16 bit Q15 numbers in Q15 representation? **(02 Marks)**

6 a. Why zero padding is done before computing the DFT? **(02 Marks)**

b. What minimum size FFT must be used to compute a DFT of 220 points in radix-2 algorithm? Determine the number of butterfly structures needed for this algorithm and thereby determine number of complex multiplications and additions needed. **(04 Marks)**

c. What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSP assembly language? **(08 Marks)**

d. Write a subroutine program to find the spectrum of the transformed data using TMS320C54XXDSP. **(06 Marks)**

7 a. Design a data memory system with address range 7FF800-7FFFFFh for a C5416 processor. Use 2K×8 SRAM memory chip. **(10 Marks)**

b. Discuss in detail the interrupt handling in the C54XX processor. **(10 Marks)**

8 a. Explain briefly the building blocks of a PCM3002 CODEC device. **(08 Marks)**

b. What do you understand by a DSP based biotelemetry receiver? **(04 Marks)**

c. With the help of block diagram, explain JPEG algorithm. **(08 Marks)**

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